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L7: Entry 1 of 5 File: USPT Oct 7, 2003

DOCUMENT-IDENTIFIER: US 6631487 B1
TITLE: On-line testing of field programmable gate array resources

Abstract Text (1):
A method of testing field programmable gate array (FPGA) resources and identifying faulty FPGA resources during normal on-line operation includes configuring an FPGA into a working area and an initial self-testing area. The working area maintains normal operation of the FPGA throughout testing and identifying of the resources. Within the initial and subsequent self-testing areas, the FPGA resources are initially tested for faults. Upon detection of a fault in the FPGA resources, the initial self-testing area resources are reconfigured or subdivided and further tested in order to identify the faulty resource. Dependent upon the further test results, the FPGA resources may be further subdivided and tested until the faulty resource is identified. Once the faulty resource is identified, the FPGA is reconfigured to replace unusable faulty resources or to avoid faulty modes of operation of partially faulty resources diagnosed during further testing. In this manner, partially faulty resources are allowed to continue operation in a diminished capacity to enhance fault tolerance. After testing each of the FPGA resources located within the initial self-testing area for faults, identifying the faulty resources, and in some instances diagnosing faulty modes of operation of the faulty resource, the FPGA is reconfigured such that a portion of the working area becomes a subsequent self-testing area and the initial self-testing area replaces that portion of the working area. In other words, the self-testing area roves around the FPGA testing its resources in a continuous manner.

Brief Summary Text (11):
On-line testing of the FPGA resources is accomplished by configuring the FPGA into a working area and an initial self-testing area. The working area maintains normal operation of the FPGA throughout testing. Within the initial and subsequent self-testing areas, however, the FPGA resources are tested for faults. It is initially presumed that all of the resources of the FPGA are fault-free as determined through manufacturing testing.

Brief Summary Text (21):
Upon completion of testing each of the FPGA resources located within the initial self-testing area, identifying the faulty resources, and diagnosing the faulty logic blocks, the FPGA under test is reconfigured so that a portion of the working area becomes a subsequent self-testing area, and the initial self-testing area, reconfigured to avoid faulty resources, becomes a portion of the working area. In other words, the self-testing area roves around the FPGA under test repeating the steps of testing and reconfiguring within the self-testing areas until each portion of the FPGA under test, is reconfigured as a subsequent self-testing area, tested, and detected faults within the FPGA resources diagnosed. As noted above, the present method of testing allows for normal operation of the FPGA under test to continue within the working area uninterrupted by the testing conducted within the self-testing areas.

Brief Summary Text (22):
An apparatus for testing the resources of the FPGA under test during normal on-line operation includes a test and reconfiguration controller in communication with the

FPGA under test for: (a) configuring the FPGA under test into an initial self-testing area and a working area, the working area maintaining normal operation of the FPGA; (b) testing the resources located within the initial self-testing area for faults; (c) reconfiguring the resources located within the initial self-testing area for further testing in order to identify the faulty resource; (d) further testing resources located within the reconfigured self-testing area; and (e) repeating the steps of reconfiguring and further testing until the faulty resource is identified. The testing apparatus further includes a storage medium in communication with the test and reconfiguration controller for storing a plurality of test configurations, and usage and fault status data for each FPGA resource.

Brief Summary Text (23):
An FPGA in accordance with the present invention includes a plurality of programmable logic blocks and a plurality of programmable routing resources interconnecting the programmable logic blocks initially configured as an initial self-testing area for testing at least a portion of the programmable routing resources and/or programmable logic blocks for faults, and an initial working area for maintaining normal operation of the FPGA during testing. The portion of the programmable routing resources and/or programmable logic blocks located within the initial self-testing area are further subdivided and tested until the faulty programmable routing resource or programmable logic block is identified.

Drawing Description Text (4):
FIG. 2 is an illustration of an FPGA under test configured into an initial self-testing area and a working area wherein the working area maintains normal operation of the FPGA under test;

Drawing Description Text (5):
FIG. 3 is an illustration of the FPGA under test configured such that the working area is divided into four disjoint areas by a vertical self-testing area and a horizontal self-testing area;

Detailed Description Text (6):
In operation, the controller 12 accesses the FPGA under test 10 in a known manner such that access is transparent to normal function of the FPGA 10. As best shown in FIG. 2, the FPGA under test 10 is initially configured by the controller 12 into an initial self-testing area 16 and a working area 18. Advantageously, this approach allows for normal operation of the FPGA under test 10 to be maintained within the working area 18 while the FPGA resources are each tested for faults in the initial self-testing area 16.

Detailed Description Text (8):
Depending upon the location of the two self-testing areas 20 and 22 at any given time during testing, the working area 18 may be contiguous, or it may be divided into two or four disjoint regions 24 as shown in FIG. 3. To accommodate testing in the self-testing areas 20 and 22, vertical wire segments in the vertical self-testing area 20 and horizontal wire segments in the horizontal self-testing area 22 are all designated reserved or unusable during operation of the FPGA under test 10. In this manner, connections between PLBs in the disjoint regions 24 of the working area 18 may be made utilizing the horizontal wire segments through the vertical self-testing area 20 and vertical wire segments through the horizontal self-testing area 22.

Detailed Description Text (22):
Upon completion of testing of each of the FPGA resources within the initial self-testing area 16, the FPGA under test 10 is reconfigured such that the functions of the PLBs forming a portion of the working area are copied to the PLBs forming the initial self-testing area 16 and appropriately re-routed. Once completed, the copied portion of the working area becomes a subsequent self-testing area. Preferably, the initial self-testing area 16 is reconfigured as an adjacent portion

of the working area, i.e., the programmed function of an adjacent portion of the working area is relocated or more specifically, copied to the initial self-testing area 16, and the adjacent portion of the working area is reconfigured as the subsequent self-testing area. The present preferred method of roving the self-testing area 16 and reconfiguring the FPGA under test 10 is described in detail in the above noted U.S. application Ser. No. 09/405,958 incorporated herein by reference.

Detailed Description Text (24):
In summary, the method of testing field programmable gate arrays in fault tolerant applications is carried out during normal on-line operation of the FPGA by configuring the FPGA resources into a working area and an initial self-testing area. The working area maintains normal operation of the FPGA throughout testing. Within the initial and subsequent self-testing areas, however, the FPGA resources are each tested and faulty resources identified by reconfiguring or subdividing and further testing the FPGA resources until the faulty resource is identified. Advantageously, the working area is substantially unaffected by testing, and testing time constraints are reduced since normal operation continues in the working area.

CLAIMS:

1. A method of testing resources of a field programmable gate array during normal on-line operation comprising the steps of: configuring said field programmable gate array into an initial self-testing area and a working area, said working area maintaining normal operation of the field programmable gate array; testing resources located within said initial self-testing area for faults; reconfiguring said resources located within said initial self-testing area for further testing in order to identify at least one resource having a fault detected during said initial testing step; further testing said resources located within said reconfigured initial self-testing area for faults; and repeating the steps of reconfiguring and testing until said at least one faulty resource is identified, whereby the field programmable gate array may be reconfigured to replace said at least one identified faulty resource in order to provide fault tolerant operation of the field programmable gate array.

15. The method set forth in claim 1, wherein the step of configuring said field programmable gate array into an initial self-testing area and a working area further includes establishing at least two testing tiles of programmable logic blocks within said initial self-testing area; and wherein said initial testing step is performed on said programmable logic blocks within said at least two testing tiles concurrently.

16. The method set forth in claim 1 further comprising the step of reconfiguring said field programmable gate array such that a portion of said working area becomes a subsequent self-testing area and at least a portion of said initial self-testing area becomes a portion of said working area.

23. An apparatus for testing the resources of at least one field programmable gate array during normal on-line operation comprising: a controller in communication with the at least one field programmable gate array for (a) configuring the at least one field programmable gate array into an initial self-testing area and a working area, said working area maintaining normal operation of the field programmable gate array, (b) testing the resources located within said initial self-testing area for faults, (c) reconfiguring the resources located within said initial self-testing area for further testing in order to identify at least one resource having a fault detected during initial testing, (d) further testing resources located within said reconfigured self-testing area, and (e) repeating the steps of (c) and (d) until said at least one faulty resource is identified.

25. A field programmable gate array comprising: a plurality of programmable logic blocks; a plurality of programmable routing resources interconnecting said programmable logic blocks; said programmable logic blocks and said programmable routing resources being initially configured as at least one initial self-testing area for testing at least a portion of said programmable logic blocks for faults, and an initial working area for maintaining normal operation of the field programmable gate array during testing; said portion of said programmable logic blocks located within said initial self-testing area being subdivided for further testing until said faulty programmable logic block is identified.

L7: Entry 2 of 5 File: USPT Jun 3, 2003

DOCUMENT-IDENTIFIER: US 6574761 B1
TITLE: On-line testing of the programmable interconnect network in field programmable gate arrays

Abstract Text (1):
A method of self-testing the programmable routing network in a field programmable gate array (FPGA) during normal on-line operation includes configuring the FPGA into an initial self-testing area and a working area. The initial self-testing area is preferably configured to include an horizontal self-testing area primarily for testing horizontal wire segments and a vertical self-testing area primarily for testing vertical wire segments. Programmable logic blocks located within the self-testing areas are configured to function as a test pattern generator and an output response analyzer, and a portion of the programmable routing resources within the self-testing areas is configured as groups of wires under test. An exhaustive set of test patterns generated by the test pattern generator is applied to the groups of wires under test which are repeatedly reconfigured in order to completely test the programmable routing resources within the self-testing areas. The outputs of the groups of wires under test are compared by the output response analyzer and resultant fault status data for each group of wires under test is received by a controller in communication with a memory for storing the fault status data. After completely testing the programmable routing resources in one of the initial self-testing areas, the FPGA is reconfigured such that a portion of the working area becomes a subsequent self-testing area and at least a portion of one of the initial self-testing areas replaces that portion of the working area. In other words, the self-testing areas rove around the FPGA repeating the steps of testing and reconfiguring until the entire FPGA has undergone testing or continuously.

Brief Summary Text (11):
In accordance with the present invention, the method of testing field programmable gate arrays (FPGAs) is carried out during normal on-line operation of the FPGA by configuring the FPGA resources into a working area and an initial self-testing area. The working area maintains normal operation of the FPGA under test throughout testing. Within the initial and subsequent self-testing areas, however, all the resources of the programmable routing network are tested. Advantageously, the working area is substantially unaffected by the testing, and testing time constraints are reduced since normal operation continues in the working area.

Brief Summary Text (18):
In accordance with an important aspect of the present invention, the self-testing area of the FPGA under test may be divided into vertical and horizontal self-testing areas. Preferably, vertical wire segments are tested utilizing the vertical self-testing area and horizontal wire segments are tested utilizing the horizontal self-testing area. To accommodate on-line testing, programmable logic blocks in both self-testing areas, vertical wire segments in the vertical self-testing area, and horizontal wire segments in the horizontal self-testing area are all designated reserved or unusable during operation of the FPGA under test. In this manner, connections between working area programmable logic blocks may be made utilizing horizontal wire segments through the vertical self-testing area and vertical wire segments through the horizontal self-testing area.

Brief Summary Text (19):
Upon completion of testing of the programmable routing resources located within the initial self-testing area, the FPGA under test is reconfigured so that a portion of the working area becomes a subsequent self-testing area, and the initial self-testing area becomes a portion of the working area. In other words, the self-testing area roves around the FPGA under test repeating the steps of reconfiguring and testing the programmable routing resources in the self-testing areas until each portion of the working area, or the entire FPGA, is reconfigured as a subsequent self-testing area and tested. As noted above, the present method of testing allows for normal operation of the FPGA under test to continue within the working area throughout testing, uninterrupted by the testing conducted within the self-testing areas.

Drawing Description Text (4):
FIG. 2 is an illustration of the FPGA under test configured into an initial self-testing area and a working area wherein the working area maintains normal operation of the FPGA under test;

Detailed Description Text (3):
A typical field programmable gate array (FPGA) generally consists of an array of programmable logic blocks interconnected by a programmable routing network and programmable input/output cells or boundary-scan ports (most FPGA's feature a boundary scan mechanism). Such structures are, for example, featured in the Lucent ORCA programmable function units, in the Xilinx XC4000 configurable logic block, and in the ALTERA FLEX 8000 logic element. In accordance with the method of the present invention, the resources of the programmable routing network of the FPGA under test are completely tested during normal operation by configuring the FPGA into a working area and a self-testing area. Advantageously, the working area is substantially unaffected by the testing conducted within the self-testing area.

Detailed Description Text (6):
In accordance with the present inventive method, the FPGA under test 10 is initially configured by the controller 12 into an initial self-testing area 16 and a working area 18 as shown in FIG. 2. The working area 18 maintains normal operation of the FPGA under test 10 throughout testing. Within the initial self-testing area 16, the resources of the programmable routing network are exhaustively tested. The programmable routing resources include both global routing resources for carrying signals amongst the array of programmable logic blocks (PLBs), and local routing resources for carrying signals into and out of the PLBs. For example, the typical global and local routing resources associated with a single PLB are shown in FIG. 3 and are discussed in more detail below.

Detailed Description Text (25):
In accordance with the present preferred method shown in FIG. 10, the initial self-testing area 16 of the FPGA under test 10 may be divided into a vertical self-testing area 80 and an horizontal self-testing area 81. The vertical self-testing area 80 is primarily utilized to test vertical routing resources or wire segments, and the horizontal self-testing area 81 is primarily utilized to test horizontal routing resources or wire segments. To accommodate operation of the FPGA under test 10 during testing, spare programmable logic blocks in both self-testing areas, horizontal wire segments in the horizontal self-testing area 80, and vertical wire segments in the vertical self-testing area 81 are all designated reserved or unusable. In accordance with an important aspect of the present invention, connections between divided working area PLBs are made utilizing horizontal wire segments through the vertical self-testing area 80 and vertical wire segments through the horizontal self-testing area 81.

Detailed Description Text (26):
Despite the advantage of continued operation during testing, the utilization of these wire segments to carry system signals through the vertical or horizontal

self-testing areas 80 and 81 between divided working area PLBs limits the ability of the self-testing areas to test cross-point CIPs. As shown in FIG. 11, the preferred method of testing cross-point CIPs 82 included in groups of WUTs 84, 86 utilizes both the vertical self-testing area 80 and the horizontal self-testing area 81. Specifically, PLBs within the horizontal self-testing area 81 are configured to include TPG 88 and PLBs within the vertical self-testing area 80 are configured to include ORA 90. The necessary test signals generated by TPG 88 are propagated along horizontal wire segments 92, 93 in the horizontal self-testing area 81, through the cross-point CIPs 82, and along vertical wire segments 94, 95 in the vertical self-testing area 80 for comparison by ORA 90.

Detailed Description Text (28):
Upon the completion of testing the programmable routing resources located within the initial self-testing area 16, the FPGA under test 10 is reconfigured such that the functions of the PLBs forming a portion of the working area 18 are copied to the PLBs forming the initial self-testing area 16. Once completed, the copied portion of the working area becomes a subsequent self-testing area. Preferably, the initial self-testing area 16 is reconfigured as an adjacent portion of the working area 18, i.e., the programmed function of an adjacent portion of the working area 18 is relocated or more specifically, copied to the initial self-testing area 16, and the adjacent portion of the working area is reconfigured as the subsequent self-testing area.

Detailed Description Text (29):
In accordance with the preferred present inventive method described above, the subsequent self-testing area may similarly be divided into vertical and horizontal self-testing areas 81 and 82 (as shown in FIG. 10) if desired. Further, the step of testing the programmable routing resources within the subsequent testing area is then repeated. This continues until each portion of the working area 18, or the entire FPGA under test 10, is reconfigured as a subsequent self-testing area and its programmable routing resources tested. In other words, the self-testing area roves around the FPGA under test 10 repeating the steps of testing and reconfiguring the programmable routing network until the entire FPGA has undergone testing. Advantageously, normal operation of the FPGA under test 10 continues uninterrupted by the testing conducted within the self-testing areas.

Detailed Description Text (31):
In summary, the method of testing field programmable gate arrays (FPGAs) is carried out during normal on-line operation of the FPGA by configuring the FPGA resources into a working area and an initial self-testing area. The working area maintains normal operation of the FPGA under test throughout testing. Within the initial and subsequent self-testing areas, however, all the programmable routing resources are exhaustively tested. Advantageously, the working area is substantially unaffected by the testing and testing time constraints are reduced since normal operation continues in the working area.

CLAIMS:

1. A method of testing programmable routing resources of a field programmable gate array during normal on-line operation comprising the steps of: configuring said field programmable gate array into an initial self-testing area and a working area, said working area maintaining normal operation of the field programmable gate array; testing said programmable routing resources located within said initial self-testing area; and roving said initial self-testing area by reconfiguring said field programmable gate array such that a portion of said working area becomes a subsequent self-testing area and at least a portion of said initial self-testing area becomes a portion of said working area.

2. The method set forth in claim 1, wherein the steps of testing and roving are repeated until each portion of said working area is reconfigured as a subsequent

self-testing area and tested.

3. The method set forth in claim 1, wherein the step of configuring said field programmable gate array into an initial self-testing area and a working area further includes configuring a first group of programmable logic blocks within said initial self-testing area to function as a test pattern generator and an output response analyzer, and a portion of said programmable routing resources within said initial self-testing area as at least two groups of wires under test.

8. The method set forth in claim 7, wherein the step of configuring said field programmable gate array into an initial self-testing area and a working area further includes configuring a second group of programmable logic blocks within said initial self-testing area to pass said test patterns there through, said second group of programmable logic blocks forming a portion of said at least two groups of wires under test, whereby local routing resources of said programmable routing resources are tested.

13. The method set forth in claim 12, wherein the steps of testing and roving are repeated until each portion of said working area is reconfigured as a subsequent self-testing area and tested.

14. The method set forth in claim 12, wherein the step of roving said initial self-testing area includes reconfiguring said field programmable gate array such that a portion of said working area becomes a subsequent horizontal or vertical self-testing area and said initial horizontal or vertical self-testing area becomes a portion of said working area.

15. A method of testing a field programmable gate array including programmable routing resources and programmable logic blocks during normal on-line operation comprising the steps of: configuring said field programmable gate array into an initial self-testing area and a working area maintaining normal operation of said field programmable gate array; applying test patterns generated by said programmable logic blocks to said programmable routing resources configured as groups of wires under test within said initial self-testing area; utilizing said programmable logic blocks to compare outputs of said groups of wires under test within said initial self-testing area; and reconfiguring said field programmable gate array such that a portion of said working area becomes a subsequent self-testing area and at least a portion of said initial self-testing area becomes a portion of said working area.

18. A method of testing a field programmable gate array including programmable routing resources and programmable logic blocks during normal on-line operation comprising the steps of: configuring said field programmable gate array into an initial horizontal self-testing area, an initial vertical self-testing area, and a working area maintaining normal operation of said field programmable gate array; applying test patterns generated by said programmable logic blocks to a portion of said programmable routing resources configured as groups of wires under test within said initial self-testing areas; utilizing said programmable logic blocks to compare outputs of said groups of wires under test within said initial self-testing areas; and reconfiguring said field programmable gate array such that a portion of said working area is utilized in forming a subsequent self-testing area and at least a portion of one of said initial self-testing areas becomes a portion of said working area.

19. The method set forth in claim 18, wherein the steps of applying test patterns, utilizing logic blocks to compare outputs, and reconfiguring are repeated until each portion of said working area is reconfigured as a subsequent self-testing area and tested.

23. An apparatus for testing programmable routing resources of a field programmable

gate array during normal on-line operation comprising: a controller in communication with said field programmable gate array for (a) configuring said field programmable gate array into an initial self-testing area and a working area, said working area maintaining normal operation of the field programmable gate array, (b) for testing said programmable routing resources located within said initial self-testing area, and (c) roving said initial self-testing area by reconfiguring said field programmable gate array such that a portion of said working area becomes a subsequent self-testing area and at least a portion of said initial self-testing area becomes a portion of said working area; and a storage medium in communication with said controller for storing a plurality of test configurations and fault status data.

24. A field programmable gate array comprising: a plurality of programmable logic blocks; a plurality of programmable routing resources interconnecting said programmable logic blocks; a plurality of input/output cells; said programmable logic blocks and said programmable routing resources being initially configured as an initial self-testing area for testing a portion of the programmable routing resources within said initial self-testing area, and an initial working area for maintaining normal on-line operation of the field programmable gate array during testing; and said programmable logic blocks and said programmable routing resources being subsequently configured as a subsequent self-testing area for testing a different portion of the programmable routing resources within said subsequent self-testing area, and a subsequent working area for maintaining normal on-line operation of the field programmable gate array during subsequent testing.